**AMENDMENTS TO THE CLAIMS:**

*This listing of claims will replace all prior versions, and listings, of claims in the application:*

1. (Currently Amended) A semiconductor integrated circuit, comprising:

a first cell comprising a plurality of transistors;

a second cell comprising a PMOS transistor section and an NMOS transistor section, the PMOS transistor section comprising a first PMOS transistor and a second PMOS transistor connected to the first PMOS transistor in series, the NMOS transistor section comprising a first NMOS transistor and a second NMOS transistor connected to the first NMOS transistor in series,

wherein a predetermined scheme is used to connect between the first cell and the second cell, between the plurality of transistors in the first cell, and between the PMOS transistor section and the NMOS transistor section in the second cell,

the first cell functions as a logic operation circuit for outputting data, and the second cell functions as a driver circuit for driving the logic operation circuit and for driving a data retaining circuit ~~for retaining~~ which retains data output by the logic operation circuit; and

wherein the first PMOS transistor and the second PMOS transistor are connected directly in series, and/or the first NMOS transistor and the second NMOS transistor are connected directly in series.

2. (Withdrawn) A semiconductor integrated circuit according to claim 1, wherein the plurality of transistors in the first cell function as at least a part of a pass transistor logic network circuit.

3. (Withdrawn) A semiconductor integrated circuit according to claim 1, wherein the predetermined scheme is a standard cell scheme or a gate array scheme.

4. (Canceled)

5. (Withdrawn) A semiconductor integrated circuit according to claim 1, wherein the plurality of transistors in the first cell include a PMOS transistor or an NMOS transistor.

6. (Original) A semiconductor integrated circuit according to claim 1, wherein the plurality of transistors in the first cell include a PMOS transistor and an NMOS transistor.

7. (Withdrawn) A semiconductor integrated circuit according to claim 1, wherein the plurality of transistors in the first cell include a transistor having a threshold higher than a predetermined value.

8. (Original) A semiconductor integrated circuit according to claim 1, wherein:

the first PMOS transistor, the second PMOS transistor, the first NMOS transistor, and the second NMOS transistor each comprise a gate, a source, and a drain;

a first source voltage is applied to the source of the first PMOS transistor;

a second source voltage is applied to the source of the first NMOS transistor;

one of the gate of the first PMOS transistor and the gate of the second PMOS transistor is connected to an input terminal, an input signal being input to the input terminal, and the other is

connected to a first gate control signal input terminal, a first gate control signal being input to the first gate control signal input terminal;

one of the gate of the first NMOS transistor and the gate of the second NMOS transistor is connected to the input terminal, and the other is connected to a second gate control signal input terminal, a second gate control signal being input to the second gate control signal input terminal; and

the drain of the second PMOS transistor and the drain of the second NMOS transistor are connected to an output terminal.

9. (Withdrawn) A semiconductor integrated circuit according to claim 8, wherein:

the gate of the first PMOS transistor is connected to the input terminal;

the gate of the second PMOS transistor is connected to the first gate control signal input terminal;

the gate of the first NMOS transistor is connected to the input terminal; and

the gate of the second NMOS transistor is connected to the second gate control signal input terminal.

10. (Withdrawn) A semiconductor integrated circuit according to claim 8, wherein:

the gate of the first PMOS transistor is connected to the first gate control signal input terminal;

the gate of the second PMOS transistor is connected to the input terminal;

the gate of the first NMOS transistor is connected to the second gate control signal input terminal; and

the gate of the second NMOS transistor is connected to the input terminal.

11. (Withdrawn) A semiconductor integrated circuit according to claim 8, wherein:

a potential of one of the first gate control signal and the second gate control signal, whichever is higher than that of the other, is higher than a potential of the first source voltage; and

a potential of one of the first gate control signal and the second gate control signal, whichever is lower than that of the other, is lower than a potential of the second source voltage.

12. (Withdrawn) A semiconductor integrated circuit according to claim 1, wherein:

a threshold voltage of one of the first PMOS transistor and the second PMOS transistor is higher than a threshold voltage of the other; and

a threshold voltage of one of the first NMOS transistor and the second NMOS transistor is higher than a threshold voltage of the other.

13. (Withdrawn) A semiconductor integrated circuit according to claim 1, wherein:

at least one transistor of the first PMOS transistor, the second PMOS transistor, the first NMOS transistor, and the second NMOS transistor is provided with a body potential terminal; and

a body potential of the at least one transistor is controlled via the body potential terminal.

14. (Withdrawn) A semiconductor integrated circuit according to claim 1, wherein:

at least one transistor of the first PMOS transistor, the second PMOS transistor, the first NMOS transistor, and the second NMOS transistor is provided with a body electrode; and

the body electrode is connected to the gate of the at least one transistor.

15. (Withdrawn) A semiconductor integrated circuit according to claim 8, further comprising:

an inverter circuit comprising the second cell,

wherein a clock signal is input to the first gate control signal input terminal or the second gate control signal input terminal.

16. (Withdrawn) A semiconductor integrated circuit according to claim 8, further comprising:

an inverter circuit comprising the second cell,

wherein a standby state control signal is input as the first gate control signal to the first gate control signal input terminal or as the second gate control signal to the second gate control signal input terminal, so that an operation of the inverter circuit is stopped in a standby state.

17. (Withdrawn) A semiconductor integrated circuit according to claim 1, further comprising:

a data retaining circuit comprising a combination of a plurality of circuits comprising the second cell.

18. (Withdrawn) A semiconductor integrated circuit according to claim 1, further comprising:

a circuit comprising the second cell,

wherein the circuit comprises a first block and a second block, and the circuit is controlled so that the first block is operated while the second block is in a standby state.

19. (Withdrawn) A semiconductor integrated circuit according to claim 8, further comprising:

a driver circuit comprising the second cell,

wherein the driver circuit is driven with the first gate control signal or the second gate control signal;

and

the gate of the first PMOS transistor, the gate of the second PMOS transistor, the gate of the first NMOS transistor, and the gate of the second NMOS transistor are connected together.

20. (Withdrawn) A semiconductor integrated circuit according to claim 3, wherein the plurality of transistors in the first cell, and the first PMOS transistor, the second PMOS transistor, the first NMOS transistor, and the second NMOS transistor in the second cell have a SOI structure.

21. (Withdrawn) A method for fabricating a semiconductor integrated circuit, comprising the steps of:

automatically synthesizing the semiconductor integrated circuit by determining a wiring pattern between a first cell comprising a plurality of transistors and a second cell comprising a PMOS transistor section and an NMOS transistor section, a wiring pattern between the plurality of transistors in the first cell, and a wiring pattern between the PMOS transistor section and the NMOS transistor section in the second cell in accordance with a predetermined scheme using a computer, wherein the PMOS transistor section comprises a first PMOS transistor and a second PMOS transistor connected to the first PMOS transistor in series, and the NMOS transistor section comprises a first NMOS transistor and a second NMOS transistor connected to the first NMOS transistor in series; and

fabricating the automatically synthesized semiconductor integrated circuit.

22. (Withdrawn) A method according to claim 21, wherein:

the predetermined scheme includes a standard cell scheme;

the first cell and the second cell are registered as standard cells in the computer; and

the step of automatically synthesizing includes using the computer to automatically synthesize the semiconductor integrated circuit by determining the wiring pattern and wiring channel width between the first cell and the second cell, the wiring pattern and wiring channel width between the plurality of transistors in the first cell, and the wiring pattern and wiring channel width between the PMOS transistor section and the NMOS transistor section in the second cell.

23. (Withdrawn) A method according to claim 21, wherein:

the predetermined scheme includes a gate array scheme; and

the automatically synthesizing step includes automatically synthesizing the semiconductor integrated circuit comprising the first cell and the second cell by using a substrate having a plurality of basic cell arrays comprising a basic cell comprising the first cell and the second cell using the computer.

24. (Canceled)

25. (New) A semiconductor integrated circuit according to claim 1, wherein the data retaining circuit comprises a data flip-flop circuit.